REMARKS

In response to the above-identified Office Action, the Applicants amend the application and seek reconsideration thereof in this response. No claims have been added. Claims 12 and 21 have been cancelled. The Applicants have amended claims 1, 8, 11, 17, 20 and 25. Accordingly, claims 1-11, 13-20 and 22-29 are pending.

The Applicants respectfully remind the Examiner that prior art rejections should ordinarily be confined strictly to the best available art (MPEP 706.02 (I) CHOICE OF PRIOR ART; BEST AVAILABLE). Merely cumulative rejections, i.e., those which would clearly fall if the primary rejection were not sustained, should be avoided. *Id.*

Claim Rejected Under 35 U.S.C. §112, First Paragraph

The Examiner rejected claim 21 under 35 U.S.C. §112, First Paragraph, as failing to comply with the written description requirement. 35 U.S.C. §112, First Paragraph, states in part:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same. . .

Elements similar to those of cancelled claim 21 appear in amended claim 20 and are addressed here. Paragraphs [0031]-[0040] of the application support the following language of amended claim 20: "transitions between the first and second modes occur upon detection by the decode unit of an ISA format boundary marker supplied by the fetch unit." The Examiner has rejected this language because the Applicants "do not discuss how one might use a file (first code) of high-level language and macroinstructions" (OA, par. 4). However, this language does not appear in amended claim 20. Specifically, the terms "source code," "file" and "high-level language" are not present in amended claim 20. Thus, the Applicants are unsure how the written description requirement has not been met, and if the Examiner maintains this rejection, the Applicants respectfully request clarification of how the written description requirement has not been met. Therefore, the Applicants respectfully request reconsideration and withdrawal of the rejection.

Claims Rejection under 35 U.S.C. §101

The Examiner rejected claims 8-10, 17-19, and 22-24 under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter.

The Applicants have amended claim 8 in response to the rejection and believe that claim 8, as amended, is directed toward statutory subject matter. Claims 9 and 10 depend from claim 8 and at least for the aforementioned reasons believe claims 9 and 10 are directed toward statutory subject matter. Therefore, the Applicants respectfully request reconsideration and withdrawal of the rejection of claims 8-10.

With respect to claims 17-19 and 22-24, the Examiner applies the printed-paper matter doctrine. However, in *In re Beauregard*, the Commissioner of Patents and Trademarks stated that he agrees with Beauregard's position on appeal that the printed matter doctrine is not applicable to *Beauregard* type claims (53 F.3d 1583 (Fed. Cir. 1995)). Claim 17 (a *Beauregard*-type claim) recites in part "A machine-readable medium having stored thereon a sequence of instructions which when executed by a processor, cause the processor to perform a method comprising: analyzing a first code; and generating a second code." Thus, the printed-paper matter doctrine is incorrectly applied to this claim because the Commissioner has found the printed matter doctrine inapplicable to these types of claims.

Claim 22 contains language similar to the aforementioned language of claim 17 and contains statutory subject matter for at least the reasons discussed in support of claim 17. Therefore, claims 17 and 22 are directed to statutory subject matter.

Claims 18, 19, 23 and 24 depend from claims 17 and 22 respectively, and are directed to statutory subject matter for at least the reasons mentioned in support of claims 17 and 22. Therefore, the Applicants respectfully request reconsideration and withdrawal of the rejection of claims 17-19 and 22-24.

Claims Rejection under 35 U.S.C. §102

Johnson

The Examiner rejected claims 1-2, 7, 17-18, 22-23, 25-26, and 28-29 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,253,308 issued to *Johnson*. The Applicants respectfully traverse the rejection of claims 22, 23, 28 and 29.

Claims 1, 2, 7, 17, 18, 25 and 26

To establish anticipation, it is axiomatic that a reference must disclose every element of the claim. With respect to amended claims 1, 17 and 25, *Johnson* fails to teach "the second code including a microarchitecture implementation-specific representation of a portion of the first code, and a macroinstruction representation of the portion of the first code."

In Fig. 10, *Johnson* discloses a functional block diagram of a retargetable cross-compiler for providing microcode programming for the intelligent controller circuit of Fig. 8. First, *Johnson* teaches compiling each portion of source code into compiler-specific language (col. 19, ll. 54-60) that includes just one representation of the source code. Second, the compiler-specific language is optimized/translated into microcode, resulting in a single version of optimized microcode (col. 19, l. 35 – col. 20, l. 11). Thus, at each compilation/translation the code is modified to create another code that contains just one representation of any portion of the prior code. Thus, Johnson fails to teach a generated code with two representations of a portion of the original code. Because *Johnson* fails to teach every element of these claims, the Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1, 17 and 25.

Claims 2, 7, 18 and 26 depend from claims 1, 17 and 25, respectively, and are patentable for at least the reasons discussed in support of their respective base claims. The Applicants respectfully request that these rejections be withdrawn as well.

Claims 22, 23, 28 and 29

With respect to claims 22, 23, 28 and 29, *Johnson* fails to teach "analyzing the first code comprising instructions for a first ISA; and generating a second code based on the first code, the second code including at least some instructions for a second ISA format corresponding to instructions in the first code." The Applicants have reviewed the reference (paying particular attention to col. 19, l. 35-col. 20, l. 11), and are unable to find where *Johnson* teaches these elements of the claims. If the Examiner maintains this rejection, the Applicants respectfully

request clarification as to what part of *Johnson* teaches or suggests generating code including instructions for an ISA different from the code it is based on.

Claims 23 and 29 depend from claim 22 and 28, respectively, and are patentable for at least the reasons discussed in support of their base claims. Therefore, the Applicants respectfully request reconsideration and withdrawal of the rejection of these claims.

Gee *et al*

The Examiner rejected claims 1-4, 7, 14-15, 17-19, 22, 23, 25, 26, 28 and 29 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,317,872 issued to Gee *et al* (*Gee*). The Applicants respectfully traverse the rejection of claims 14, 15, 22, 23, 28 and 29.

Claims 1-4, 7, 17-19, 25 and 26

With respect to amended claims 1, 17 and 25, *Gee* fails to teach "the second code including a microarchitecture implementation-specific representation of a portion of the first code, and a macroinstruction representation of the portion of the first code." *Gee* teaches optimized execution of JAVA™ programs. *Gee* makes use of a real time processor that is optimized for executing JAVA™ programs (col. 2, ll. 42-51). Compilation of the source code results in code known as bytecode. *Id.* The bytecode contains only one representation of the source code.

Gee teaches a JAVA™ embedded microprocessor (JEM) that is a microprogrammed machine where program control is carried out via stored program (on ROM) rather than discrete sequential logic (col. 8, ll. 34-40). The source code (JAVA™) is compiled into an intermediate code (bytecode) that is stored in ROM 200. The microprocessor system then selects and executes the native level code from ROM 104 in response to the intermediate code. "In essence, each bytecode is interpreted as a pointer to a sequence of microinstructions which will actually be executed in place of the bytecode" (col. 8, ll. 49-62). Therefore, *Gee* teaches compiled code and execution codes that contains only one representation of the original code. Thus, the cited claim language is patentably distinct over the reference because the reference teaches a second code containing just a single representation while the claims recite that the second code contains both "a microarchitecture implementation-specific representation" and "macroinstruction representation."

Because *Gee* fails to teach every element of these claims, the Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1, 17 and 25. Claims 2-4, 7, 18, 19 and 26 depend from claims 1, 17 and 25, respectively, and are patentable for at least the reasons discussed in support of their base claim. The Applicants respectfully request that these rejections be reconsidered and withdrawn as well.

Claims 14, 15, 22, 23, 28 and 29

With respect to claims 14, 22 and 28 *Gee* fails to teach "a first code comprising instructions for a first ISA; and . . . [a] second code including at least some instructions for a second ISA." *Gee* teaches that the compiled and optimized code contains instructions for a single instruction set architecture (ISA) referred to in the disclosure as the JEM architecture. The JEM architecture is based upon improvements to the Rockwell Advanced Architecture Microprocessor. See col. 11, ll. 32-50. However, all of the code in *Gee* is for a single architecture - the JEM architecture and not the Rockwell Advanced Architecture. Thus, *Gee* teaches code for a single architecture – the JEM architecture. Because *Gee* fails to teach a first and second ISA, claims 14, 22 and 28 are patentably distinct from *Gee*.

Therefore, *Gee* fails to teach every element of these claims, and the Applicants respectfully request reconsideration and withdrawal of this rejection. Claims 15, 23 and 29 depend from claims 14, 22 and 28, respectively, and are patentable for at least the reasons discussed in support of their base claims. The Applicants respectfully request that these rejections be reconsidered and withdrawn as well.

Bullions III *et al*

The Examiner rejected claims 1-7, 11-15, 17-23, 25, 26, 28 and 29 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,280,593 issued to Bullions, III *et al* (*Bullions*). The Applicants respectfully traverse the rejection of claims 22, 23, 28 and 29.

Claims 1-7, 17-19, 25 and 26

Bullions fails to teach "generating a second code based on the first code, the second code including a microarchitecture implementation-specific representation of a portion of the first

code, and a macroinstruction representation of the portion of the first code" as recited in amended claims 1, 17 and 25.

Col. 5, ll. 23-26 recite that milli-routines consist of a mixture of regular System 390 instructions and private milli-mode only instructions. *Bullions* teaches that these routines are stored in Millicode Array 108 (col. 5, ll. 20-23). *Bullions* fails to teach that these routines contain "microarchitecture implementation-specific representation of a portion of the first code, and a macroinstruction representation of the portion of the first code." Instead, the routines contain only one representation of any single portion of the source code, either as regular System 390 instructions or as private milli-mode only instructions.

Because *Bullions* fails to teach every element of these claims, the Applicants respectfully request reconsideration and withdrawal of the rejection. Claims 2-7, 18, 19 and 26 depend from claims 1, 17 and 25, respectively, and are patentable for at least the reasons discussed in support of their base claim. The Applicants respectfully request that these rejections be withdrawn as well.

Claims 14, 15, 22, 23, 28 and 29

With respect to claims 14, 22 and 28, *Bullions* fails to teach "a first code comprising instructions for a first ISA; and . . . [a] second code including at least some instructions for a second ISA." *Bullions* teaches the IBM System 390 architecture in an exemplary embodiment (see figure 1 and col. 4, ll. 48-59) and adds that other IBM or non-IBM architectures may be used alternatively. See figure 1 and col. 4, ll. 48-59. However, these alternative architectures are meant as alternatives for the exemplary System 390 architecture, meaning that they would be used instead of, and not in conjunction with, the System 390 architecture. The selected ISA may be any one of System 390, IBM or non-IBM architectures, but once an ISA is selected, no other ISA is used. Therefore, *Bullions* fails to teach "[a] second code including at least some instructions for a second ISA."

Because *Bullions* fails to teach every element of these claims, the Applicants respectfully request reconsideration and withdrawal of this rejection. Claims 15, 23 and 29 depend from claims 14, 22 and 28, respectively, and are patentable for at least the reasons discussed in

support of their base claims. The Applicants respectfully request that these rejections be withdrawn as well.

Claims 11, 13 and 20

With respect to amended claims 11 and 20, *Bullions* fails to teach "an ISA format boundary marker." Instead, *Bullions* teaches a milli-instruction (col. 8, ll. 66-68). Because milli-instructions are patentably distinct from ISA instructions, *Bullions* fails to teach the cited language.

The Examiner equates instructions that are to be interpreted in milli-mode with "an ISA format boundary marker" (OA, par. 14, *Bullions*, col. 6, ll. 7-9). In *Bullions*, instructions that are to be interpreted in milli-mode are called milli-instructions (col. 5, ll. 21-29). However, *Bullions* teaches that instructions that are interpreted in milli-mode are not of the ISA format. Rather, they are unique, private (unknown to the user) milli-instructions that are implementation specific, while ISA instructions are known to the user (col. 6, ll. 16-19; col. 5, ll. 21-29; see Abstract, Glossary).

Thus, *Bullions* teaches that a milli-mode instruction is not equivalent to an ISA instruction or ISA format boundary marker. Therefore, *Bullions* fails to teach an ISA format boundary marker. Because *Bullions* fails to teach every element of these claims, the Applicants respectfully request reconsideration and withdrawal of this rejection.

Claim 13 depends from claim 11 and is patentable for at least the reasons discussed in support of the base claims. The Applicants respectfully request that this rejection be withdrawn as well.

Brown *et al*

The Examiner rejected claims 14-16 and 22-24 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,537,629 issued to Brown *et al* (*Brown*). The Applicants respectfully traverse this rejection.

With respect to claims 14 and 22, *Brown* fails to teach "analyzing a first code comprising instructions for a first ISA; and generating a second code based on the first code, the second

code including at least some instructions for a second ISA corresponding to instructions in the first code."

Brown teaches a decoder for single cycle decoding of single prefixes in a variable length instruction. Although *Brown* teaches "that the structures described herein could also be used with instruction sets other than the INTEL instruction set," *Brown's* embodiments are all carried out in the context of a single instruction set architecture (col. 4, ll. 37-48). *Brown* teaches use of a single instruction set architecture throughout the process of compiling (col. 1, ll. 42-67). Therefore, *Brown* fails to teach mixing a first and a second ISA during code generation. Because *Brown* fails to teach every limitation of the cited claim language, the Applicants respectfully request reconsideration and withdrawal of the rejection of these claims.

Claims 15, 16, 23 and 24 depend from claims 14 and 22, respectively, and are patentable for at least the reasons discussed in support of the base claims. The Applicants respectfully request that these rejections be withdrawn as well.

CONCLUSION

In view of the foregoing, the Applicants believe that all claims are now in condition for allowance and the Applicants earnestly solicit such action at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: June 27, 2006

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Susan M. Barrette — June 27, 2006